

John W. Kesterson

John is the founder and president of AISD, inc. He formed the company as a sole proprietorship in June 1995 to provide custom DSP firmware and software solutions to the telecommunications industry. The company was formed into a corporation in April of 2000. John is an experienced design engineer with experience in military and commercial communications systems, DSP implementations of many standards, spread spectrum navigation and communications systems, acoustic and audio signal processing as well as geophysical signal processing giving him a deep understanding of algorithm development, code development and systems integration.

Summary of Work Experience

Skilled in Analog and Digital Signal Processing Development, and algorithm development, Verilog HDL and Xilinx synthesis, DSP hardware modeling, system and media modeling, analog and digital filter design, linear and non-linear loop analysis, adaptive learning algorithms. Experienced with many RF, and telephony modem communications, media (cable, RF, and telephony, CAT-5, CAT-6) systems, and model development and characterizations. Experienced with bi-Static RADAR, Spread Spectrum (Nav and Comm), and TDMA, CDMA, FDMA systems.

Skills/Strengths

- Verilog HDL system modeling, simulation, synthesis and RTL translation.
- Algorithm porting to synthesizable Verilog.
- C++/C, Pascal, FORTRAN, VB and Verilog HDL.
- DSP Modeling, Embedded Systems, Porting Code.
- Intel, Motorola, TI and DSP Group DSP processors.
- Unix, Linux, DOS, Windows
- SimulCAD, Cadence(Digital and Analog), Synopsys, Synplicity, MathCad EDA tools.
- Telemetry Applications.
- Xilinx and Altera FPGAs, CPLDs, PLDs.
- Strong Problem Solving and Troubleshooting Skills.

Work and Experience History

6/95 - Pres. - **Absolute Integrated Systems Developers**, Grass Valley, CA
President/Consulting Engineer - Operates small consulting and development business providing signal processing solutions to customers in wireless, telephony and Ethernet modems as well as other electronic control and monitor systems. Other developments include down hole media channel model development, Custom modem architecture designs for unique media (down hole through drilling pipe), system level architecture design, channel and cable model

developments, Measurement while drilling real time FFT processing and display client server display tools under Windows, Ethernet phy designs (including Gigabit), a LASER pointing servo control system for ophthalmology, a vehicular dynamometer micro-controller development and a resistivity meter for a geophysical prospecting company. Project developments include hard, soft and firmware developments. Extensive experience with micro-controller and DSP development. Manages efforts of subcontractors and employees.

9/91 - 5/95 - **Mitsubishi Electronics America R & D Center**, Nevada City, CA - **Senior Electronics Engineer** - Developed direct sequence spread spectrum system ASIC for wireless communications systems. Developed digital modulator and demodulator implementations using custom DSP architectures which include digital filters and differential encoder and decoders for both BPSK and QPSK. Developed an all digital maximum likelihood clock and data recovery loop which works with sampled NRZ data. Also developed 915 MHz RF system and 70/10.7 MHz IF system prototype. This was for ASIC testing as well as development into a mixed signal custom IC. Development work was done using Synopsys and Cadence EDA tools on Sun Sparc platform. Digital subsystems were prototyped using Xilinx FPGA's.

4/90 - 9/91 **Galaxy Microsystems**, Austin, TX - **Program Manager** - Led development effort on Ground Wave Spread Spectrum Position Location (PL) system for Ft. Hood weapons systems evaluation system. Supervised 3 engineers and 2 technicians and coordinated efforts of several independent consultants. System also included a VHF/UHF TDMA radio data link. The PL system is a direct sequence CDMA spread spectrum which provides time difference of arrival information used in a hyperbolic navigation algorithm to determine position within 1 meter accuracy in a 100 square kilometer area.

9/89 - 4/90 **Crystal Semiconductor Corporation**, Austin, TX - **Senior Test Development Engineer** - Developed an automated test solution for the 8392 Ethernet Tap chip. Test system included development of a wave form digitizer capable of measuring rise and fall times in the 25 nsec domain with .1 nsec accuracy and 10 psec resolution. Also worked in the development of a generalized test solution for delta-sigma A/D converters. Optimized Delta Sigma ADC test loop for the internal filter response of the chip reducing the test time from 95 seconds to less than 25 seconds.

7/87 - 9/89 **Advanced Energy Technology**, Austin, TX - **Engineering Manager** - Team Leader for Electromagnetic Array Profiling (EMAP-1) system development. EMAP-1 is an electrical methods geophysical prospecting tool. Supervised three hardware and two software engineers. Coordinated efforts of several independent consultants. Was involved in all phases of the design as one of the system architects. Design included analog signal conditioning, DSP software, and field sensors. Designed analog instrumentation amplifiers, filters, cable drivers for remote sensors and software for signal processing.

9/84 - 7/87 **Tracor Applied Sciences**, Austin, TX - **Project Engineer/Scientist** -
Joined group to develop Passive Aircraft Detection and Identification System (PADIS), a secondary bi-static RADAR receiver which monitors the ground interrogator activity as well as aircraft beacon replies. The system computes flight tracks from the received data using a bi-static tracking algorithm. Developed system concept, designed a prototype system, wrote software for the system, and integrated the system with an existing noise monitoring system at San Francisco International Airport.

3/82 - 9/84 **Geotronics Corporation**, Austin, TX - **Research Engineer** -
Employed as an associate engineer in manufacturing; later transferred to R&D engineering group as a research engineer. Developed recording and processing systems. Performed system characterizations used in data processing software. Performed software development in C on Unix.

6/72 – 3/82 - **U.S. Air Force - Electronics Technician and Technical Instructor**

Education

Bachelor of Science in Electrical Engineering, 1983 - Columbia Pacific University at San Rafael, CA

Numerous courses from UCSD Extension in DSP algorithm development, chaos theory, neural networks, and adaptive learning algorithms.

George Washington University Extension in Spread Spectrum Systems
Cadence Verilog, Spice, and AWB EDA tools courses.

Professional/Technical Associations

Member, Institute for Electrical and Electronics Engineers

Member, IEEE Acoustics, Speech, and Signal Processing Society

Member, IEEE Neural Networks Society

Publications

IEEE Custom Integrated Circuits Conference – Educational Session May 21, 2000 on Modem Fundamentals. Presented two hour educational session on DSP and its use in Modem designs.

Relative Phase Modeling Approach to Loop Simulation. Describes simulation method for complex loop systems containing a wide dynamic range of frequencies using relative phase vs. time instead of voltage and current vs. time. Published in EDN magazine Nov. 11, 1993.

IIR Filter Simplified Architecture. This white paper describes a simplified

architecture for implementing first and second order IIR filters in communications systems. The number of gates used in the design is reduced such that several of them can be installed in a single 20,000 gate ASIC to implement DSP functions at Intermediate Frequency speeds.

Co-authored data sheet for SSTM001 data sheet. This data sheet describes in detail the operation of the Spread Spectrum Technology Modem ASIC (SSTM001) developed at Mitsubishi R&D Center, Nevada City, CA.

Cable Response using Lumped Parameter Chain Matrix. Describes algorithm for correction of cable transmission line effects of seismic type cable used to record EM data over a wide frequency range. An internal document at AET/Geotronics.

Possible Errors in Power Averages Based on Messages Sent in dB. Appendix 1 to Tracor proposal to Edmonton Airport for Tracor Noise Monitoring System. This paper is a statistical analysis of the overall effect of errors in power averages that are sent in dB on the overall average.

Forward Looking Radar Synthetic Reply Test Set, Patent disclosure for equipment developed for evaluating RADAR performance of terrain following, forward looking radar. U.S. Patent 4,499,469 February 12, 1985.